



# Review of Test Circuits TX and TY

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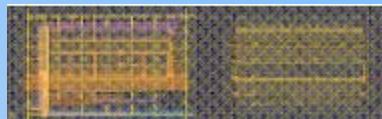
# TX and TY

- Two areas on MPW run #1 were specifically allocated to test structures (TX & TY).
- Each chip is 6.3 x 2.0 mm
- Some devices on the chips can be tested either as a 2D device or as a 3D structure.
- These test chips are available to all members of the consortium for testing. (We encourage others to take some chips and share results.)
- This presentation should allow for testing the chips.

# Test Chips TX & TY Summary



TX Left



TX Right

## •Subreticule TX

- 1) **Test transistors** for noise, radiation, and cryo measurements
  - 1) NMOS and PMOS transistor array with nominal  $V_t$ , low  $V_t$ , thick gate oxide I/O, 0  $V_t$ , and 0  $V_t$  thick gate oxide. **Measured devices are thinned.** (PAVIA)
  - 2) NMOS and PMOS transistor array with different numbers of fingers/transistor for measurements at cryo temperatures. **Devices can be measured on thick or thin substrate.** (FNAL)

- 2) **Test circuits for VIP2b** in subreticule I - (FNAL)

- Double correlated sampler
- Single channel FE
- Front ends with different W/L input transistors
- Stand alone discriminator



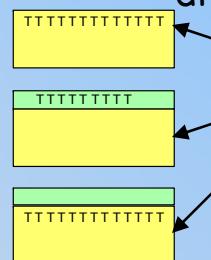
TY Left



TY Right

## •Subreticule TY - (FNAL)

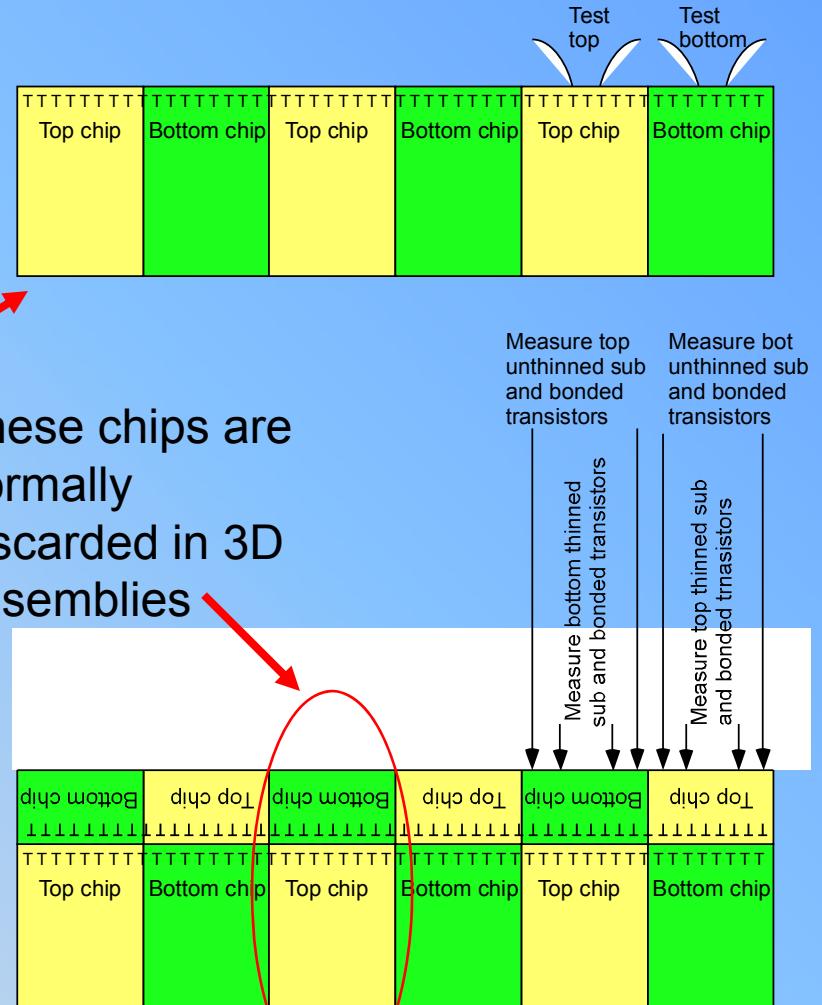
- 1) **Two long daisy chains** of bond interconnects to measure interconnect yield.
  - Two different daisy chains having different bond interface patterns
  - Each daisy chain has 140000 bond interconnects with multiple taps
- 2) **Test transistors** based on a standard set of devices (~46) used by CERN to characterize different processes.
  - Devices can be measured under different conditions



- on standard wafers (2D wafers).
- on thin substrate bonded to a thick second wafer
- on thick substrate bonded to a thinned second wafer.

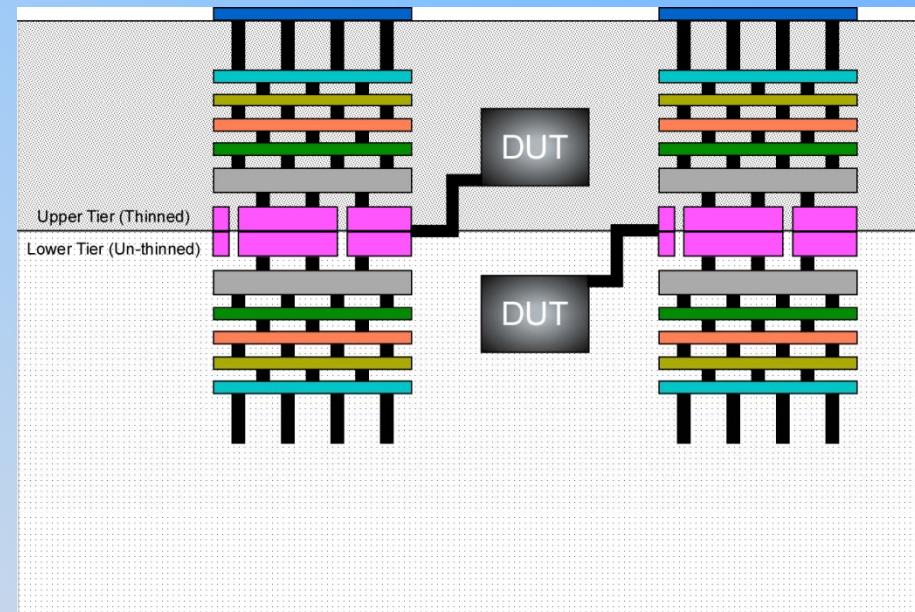
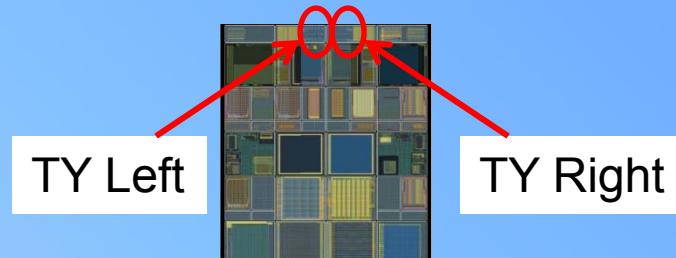
# 2D and 3D Testing

- Initially most test structures except daisy chains were to be measured on 2D wafers.
- To do this 2D wafers are pulled from the line and pads placed on top for measurements
- After some thought, it was realized that test transistors could be measured in two ways on 3D wafers to provide additional information.
- In fact devices could be measured on both the thick and thin substrates.
- How is this done?

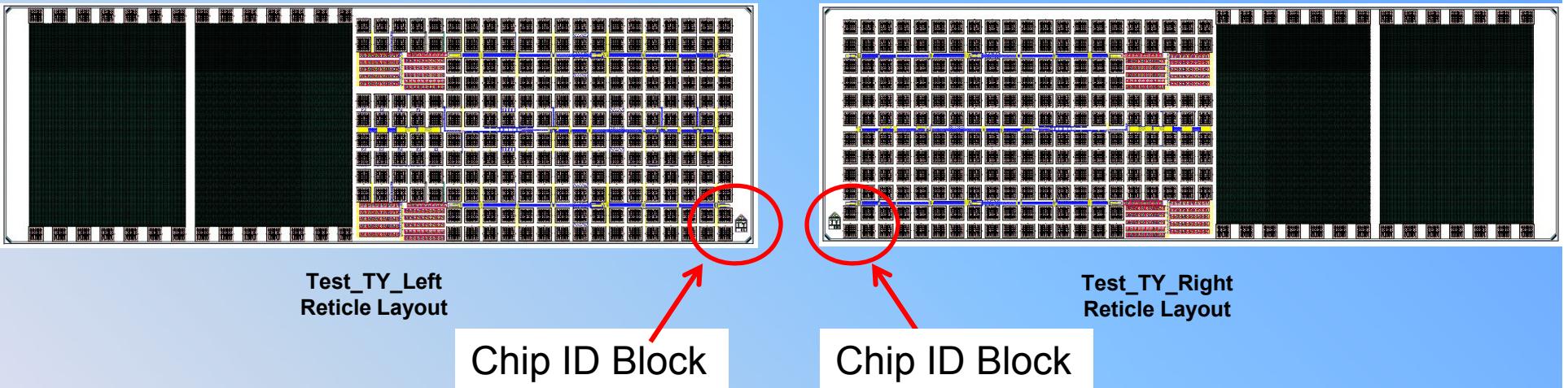


# Side-by-side Double Stack Pads

- With special pads.
- To the right is the final reticule
- Consider test chip TY as an example
- TY is at the top of the reticule (highlighted)



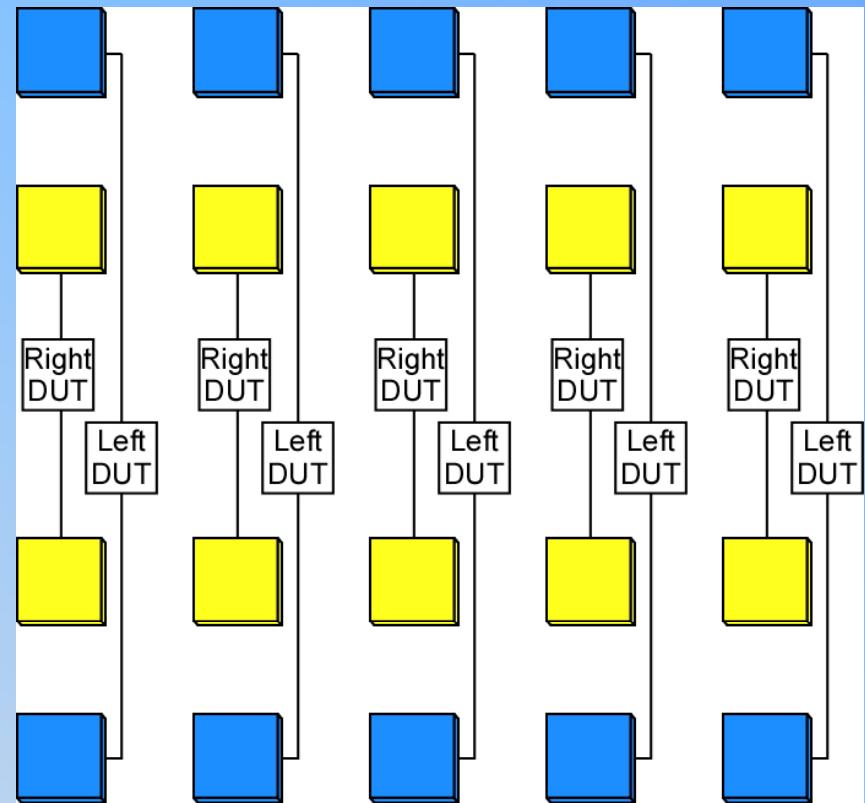
# Side-by-side Double Stack Pads



- When you get a TY test chip in a 3D chip, the Chip ID block will either be on the left or the right depending on which chip you get.
- Remember, a 3D stack is created by taking 2 wafers, flipping one of them and aligning them on top of one another. The one on top has been thinned to reach the TSVs.
- So which one is on top in YOUR chip?
  - When the Chip ID block is on the right, then Test\_TY\_Right is on top.
    - Therefore the circuit elements in Test\_TY\_Right have been thinned.
  - When the Chip ID block is on the left, then Test\_TY\_Left is on top.
    - Therefore the circuit elements in Test\_TY\_Left have been thinned.

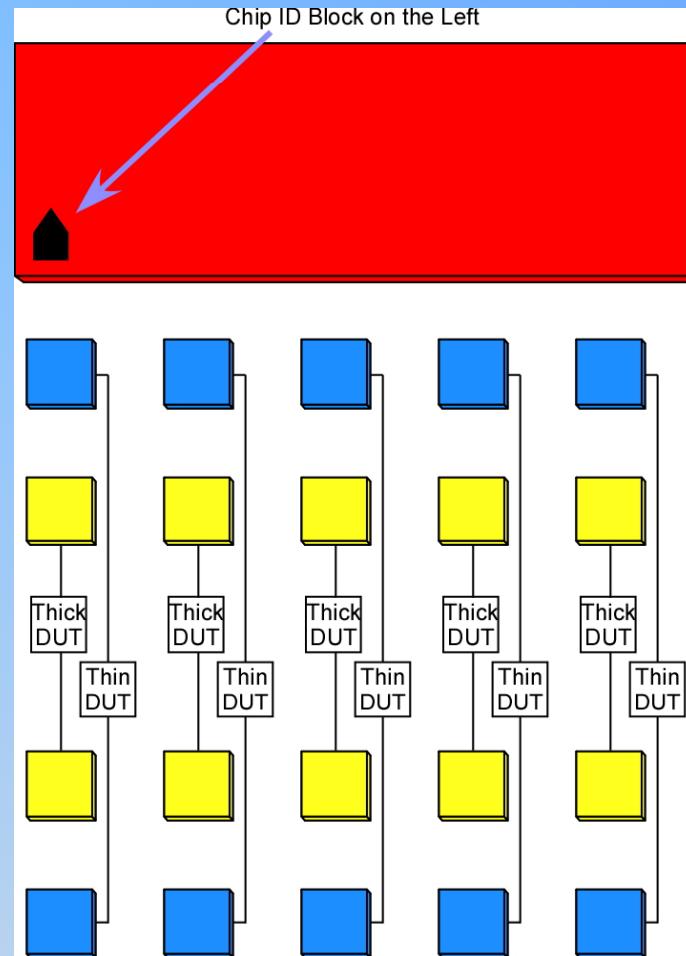
# Side-by-side Double Stack Pads

- How were the pads arranged?
- To the right is a mock-up of the pad structure showing the general idea.
- Identical test circuit elements are placed in the same (X,Y) locations on both Left and Right Tiers.
- Left Tier circuit elements are connected to "outer" pads
- Right Tier circuit elements are connected to "inner" pads



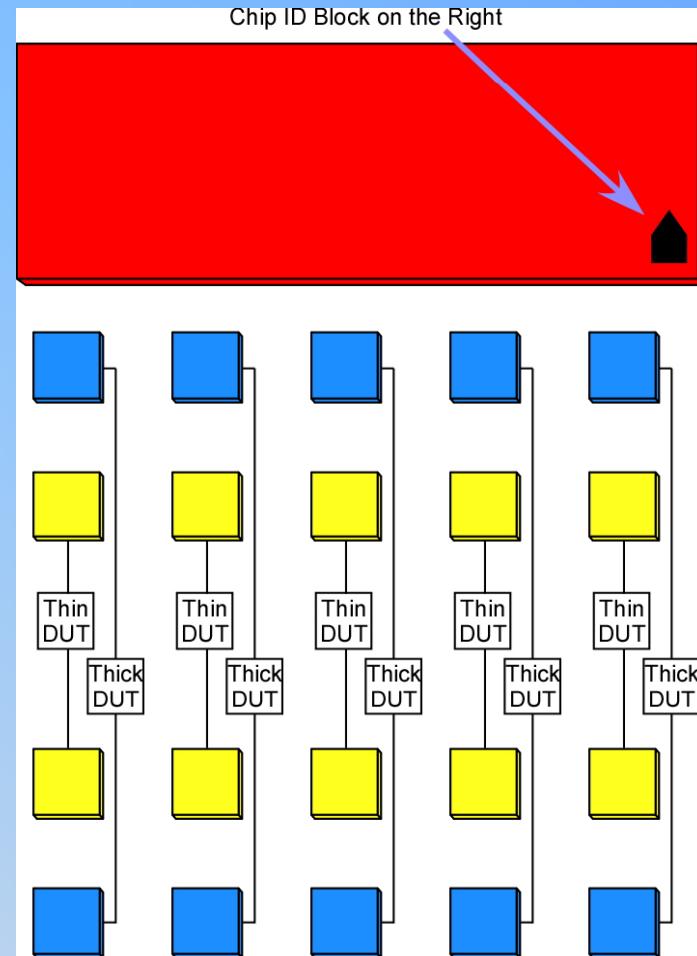
# Side-by-side Double Stack Pads

- In the case of a TY 3D stack with the chipID block on the **left**, then the **left** Tier is on top and therefore the **left** Tier circuit elements have been subjected to thinning
- The pads, in general, would be as shown here.



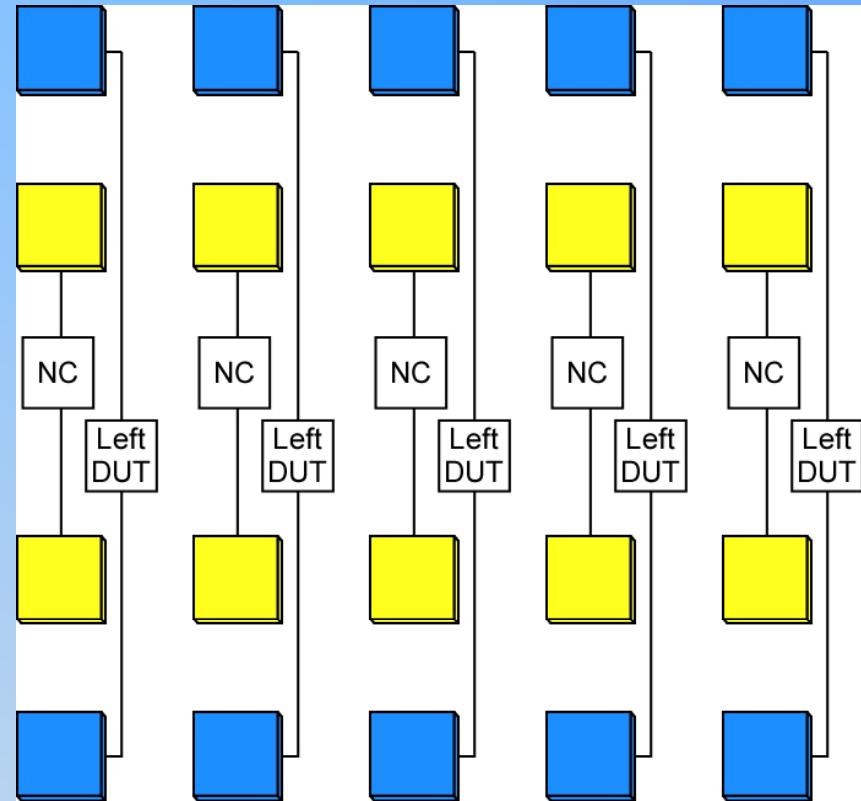
# Side-by-side Double Stack Pads

- In the case of a TY 3D stack with the chipID block on the **right**, then the **right** Tier is on top and therefore the **right** Tier circuit elements have been subjected to thinning
- The pads, in general, would be as shown here.



# Side-by-side Double Stack Pads on the 2D Test Wafers

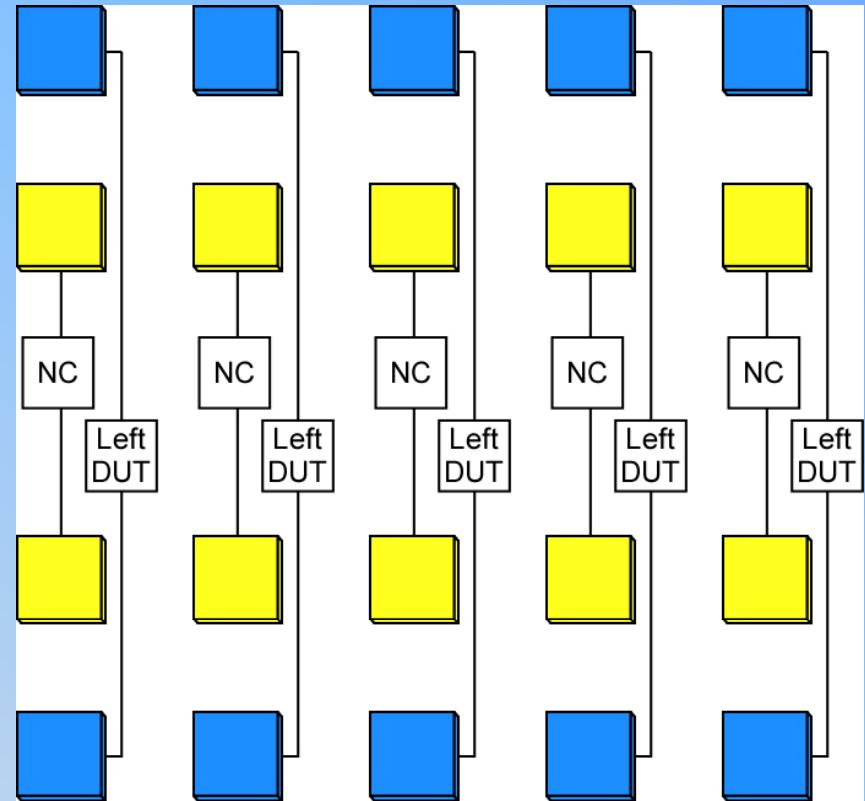
- In the case of a TY 2D test chip with the chipID block on the **left**, then you are looking at the **right** Tier.
- The pads, in general, would be as shown here.



2D Test Wafers Only!!!

# Side-by-side Double Stack Pads on the 2D Test Wafers

- In the case of a TY 2D test chip with the chipID block on the **right**, then you are looking at the **left** Tier.
- The pads, in general, would be as shown here.

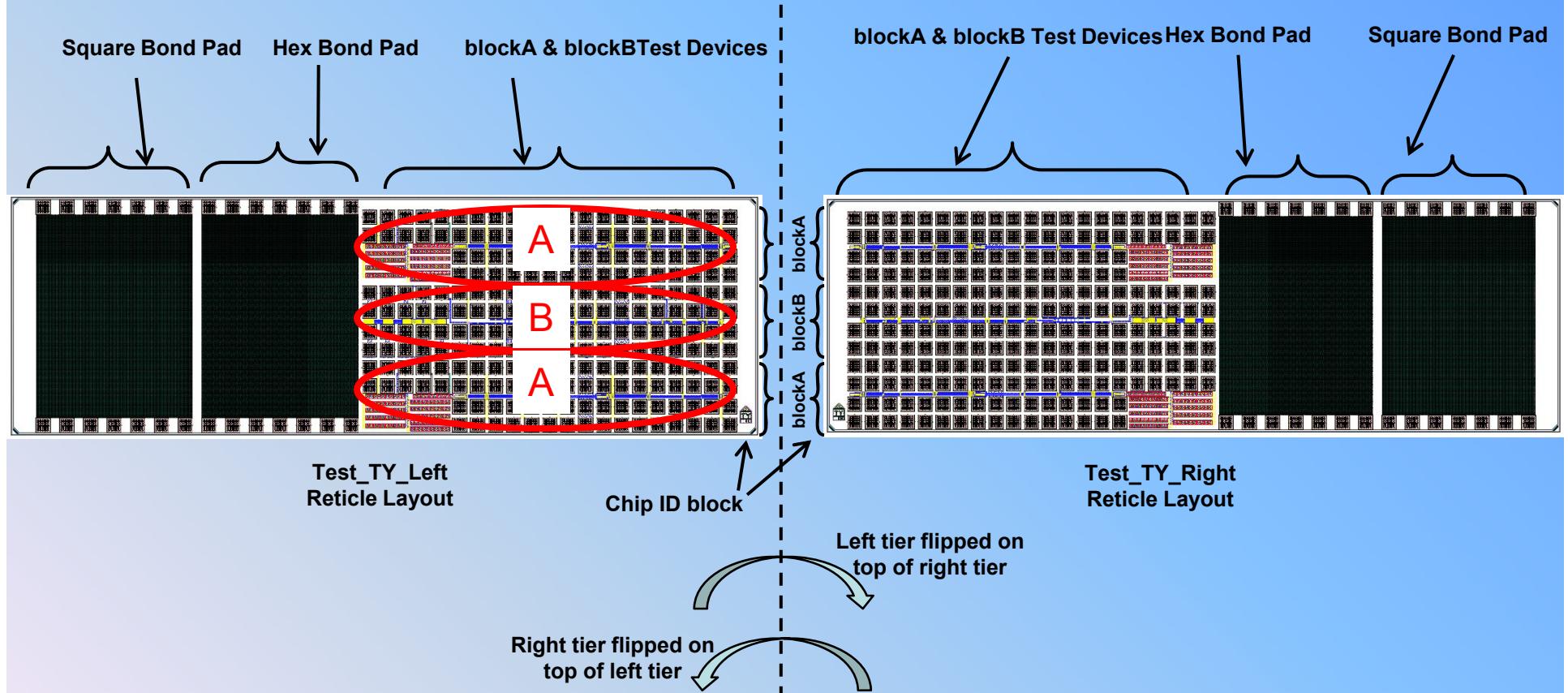


2D Test Wafers Only!!!

# Test Chip TY

- Contains two different bond interface daisy chains with 140,000 bond interfaces to test yield.
- Contains the “standard” set of test transistors used by CERN for characterization of various 0.13 um processes.

# Test TY (FermiLab Test Chip Y)

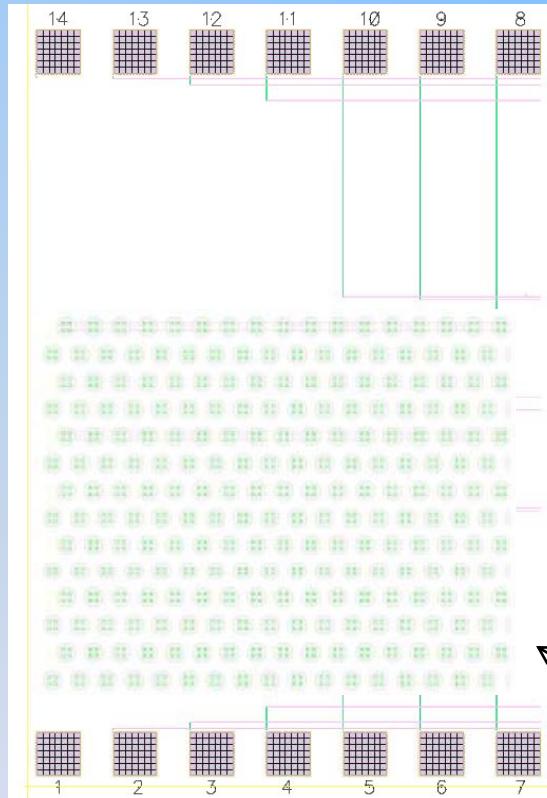


## Via and Bond Pad Daisy Chain

330 x 426 array bond pads on 4 um pitch. 3D testing is possible only on  
The top (thinned) tier.

## FermiLab Test Devices

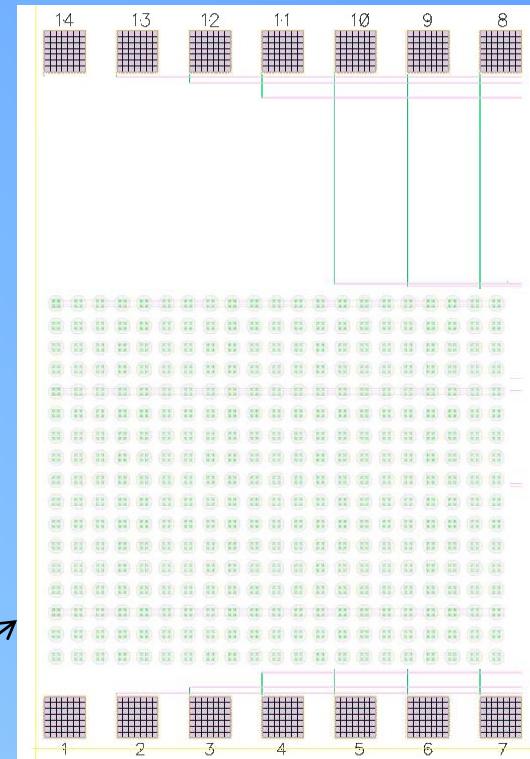
2D & 3D testing is possible



## Daisy Chains (Hex & Square Pad Pattern)

Two different patterns  
Are being tested

Hex and Square bond pattern only partly shown

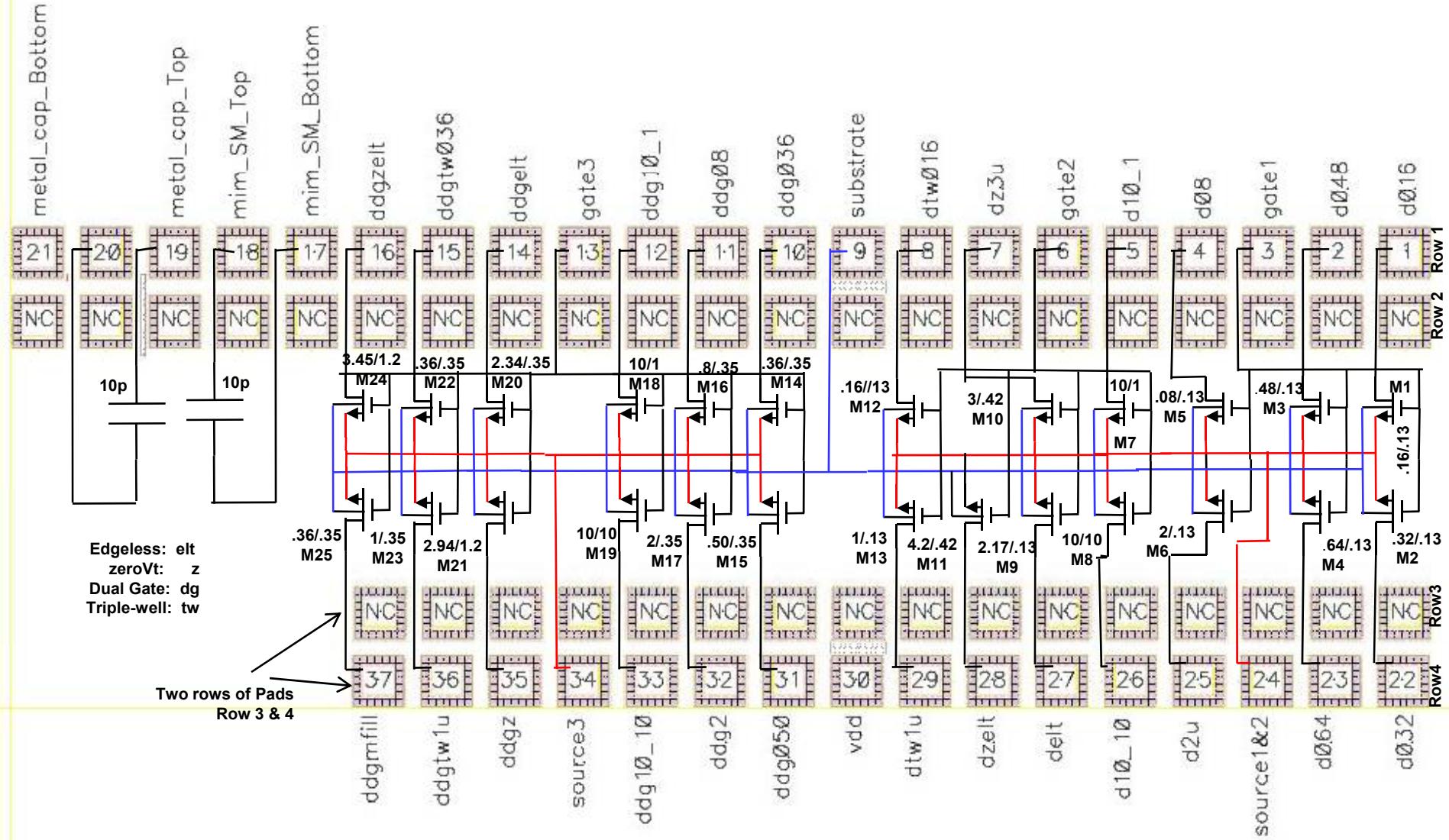


<b>Pin#</b>	<b>Row</b>	<b>Pad</b>
1	1	1
2	1 <sup>st</sup>	330 <sup>th</sup>
3	5 <sup>th</sup>	1650 <sup>th</sup>
4	15 <sup>th</sup>	4959 <sup>th</sup>
5	143 <sup>rd</sup>	47190 <sup>th</sup>

<b>Pin#</b>	<b>Row</b>	<b>Pad</b>
6	145 <sup>th</sup>	47850 <sup>th</sup>
7	209 <sup>th</sup>	68970 <sup>th</sup>
8	217 <sup>th</sup>	71610 <sup>th</sup>
9	281 <sup>st</sup>	92730 <sup>th</sup>
10	283 <sup>rd</sup>	93390 <sup>th</sup>

<b>Pin#</b>	<b>Row</b>	<b>Pad</b>
11	411 <sup>th</sup>	135630 <sup>th</sup>
12	421 <sup>st</sup>	138930 <sup>th</sup>
13	425 <sup>th</sup>	140250 <sup>th</sup>
14	426 <sup>st</sup>	140589 <sup>th</sup>

## Test\_TY\_Left (blockA) 2D View

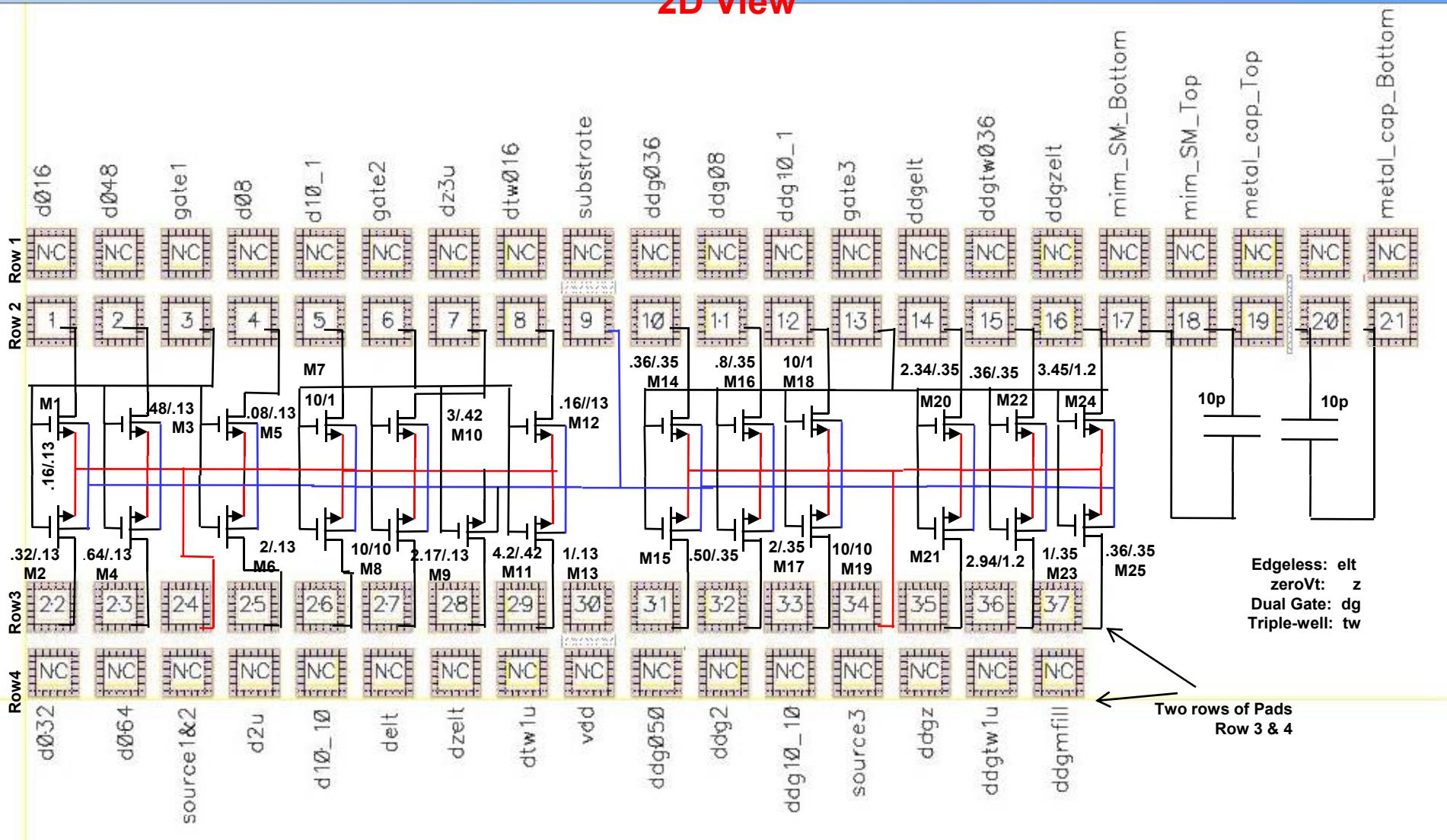


The blockA(Test\_TY\_Left) is 2D layout shown above which contains 37 pads. NC means no connection. There are four rows of pads. In 2D layout, row 2 and 3 are not connected(NC) to any devices. Only row 1 and 4 are connected to devices. blockA consists of nmos, ZeroVt(z) nmos, dual Gate(dg) nmos, edgeless(elt) nmos, triple-well(tw)nmos, dgelt nmos, dgtw nmos, dazelt nmos transistors, and 2 capacitors.

**Protection diodes at the gates are shown in the above layout. Vdd is connected to protection diode.**

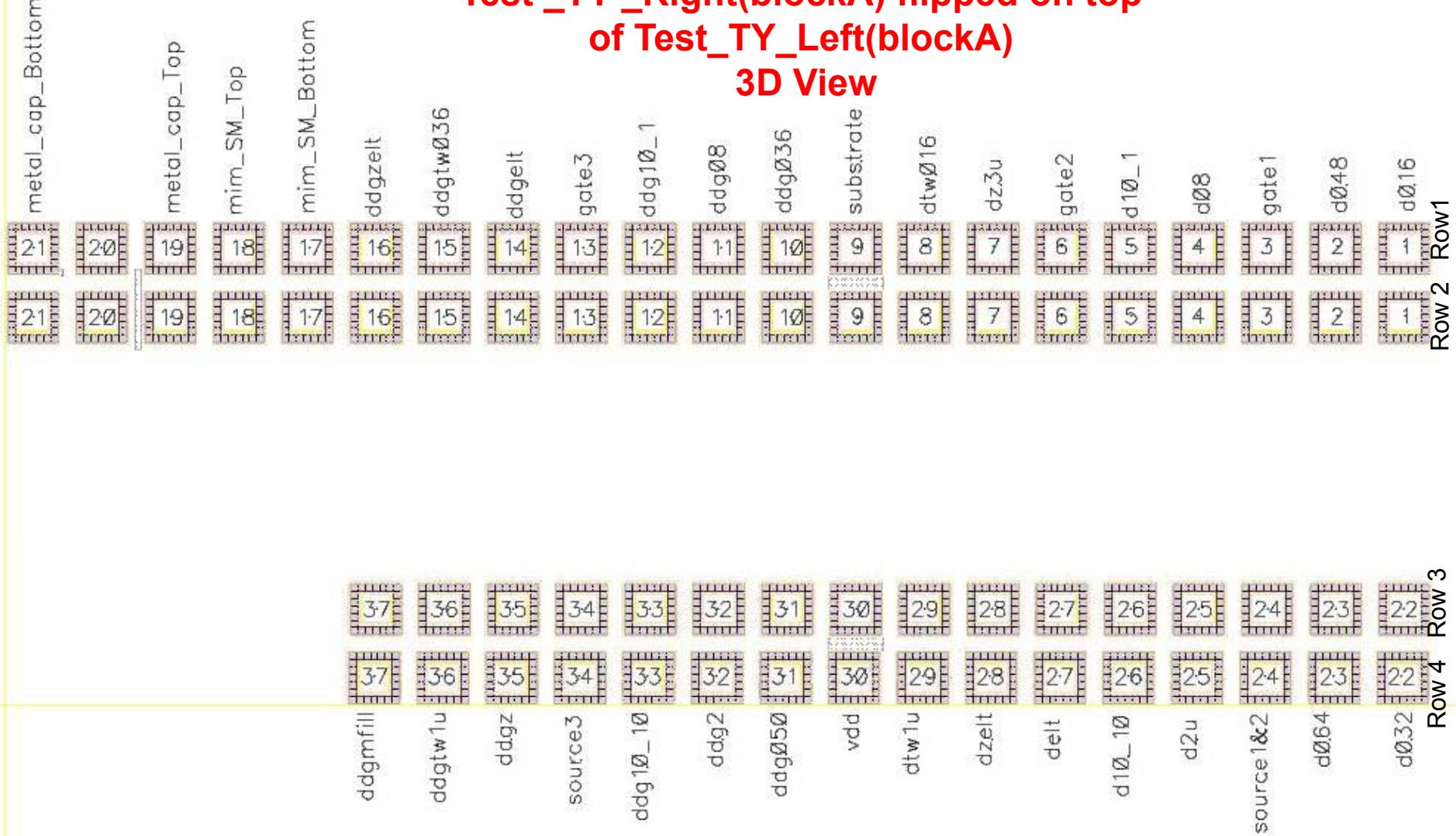
# Test\_TY\_Right (blockA)

## 2D View



The blockA(Test\_TY\_Right) is 2D layout shown above which is mirror of blockA(Test\_TY\_Left). In this layout, row 2 & 3 are connected to devices and unconnected rows are 1 & 4. NC means no connection. Pin name & devices are exact same as blockA(Test\_Ty\_left). blockA consists of nmos, ZeroVt(z) nmos, dual Gate(dg) nmos, edgeless(elt) nmos, triple-well(tw)nmos, dgelt nmos, dgtw nmos, dgzelt nmos transistors, and 2 capacitors. Protection diodes at the gates are not shown in the above layout. Vdd is connected to protection diode.

## Test\_TY\_Right(blockA) flipped on top of Test\_TY\_Left(blockA) 3D View



3D layout of blockA is shown above . where right tier flipped on top of left tier which means row of 1 & 4 pads are connected to circuit. In the case of left tier flipped on top of right tier then row of 2 & 3 are connected to circuit. Either 17 case, one can test the circuit by accessing row 1 & 4 or row 2 & 3. Note that chip ID will be on right side corner.

**Test\_TY\_Left(blockA) flipped on top  
of Test\_TY\_Right(blockA)  
3D View**

Row 2 Row 1	d@16	d@48	gate1	d@8	d1@_1	gate2	dz3u	dtw@16	substrate	ddg@36	ddg@8	ddg@1@_1	ddg@3	ddgelt	ddgtw@36	mim_SM_Bottom	mim_SM_Top	metal_cap_Top	metal_cap_Bottom
Row 2 Row 1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Row 3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Row 4 Row 3	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37			
Row 4 Row 3	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37			
	d@32	d@64	source1&2	d2u	d1@_10	deit	dzelt	dtw@1u	vdd	ddg@50	ddg2	ddg@1@_10	source3	ddgz	ddgtw@1u	ddgffill			

3D layout of blockA is shown above . where left tier flipped on top of right tier which means row of 2 & 3 pads are connected to circuit. In the case of right tier flipped on top of left tier then row of 1 & 4 are connected to circuit. Either 18 case, one can test the circuit by accessing row 1 & 4 or row 2 & 3. Note that chip ID will be on left side corner.

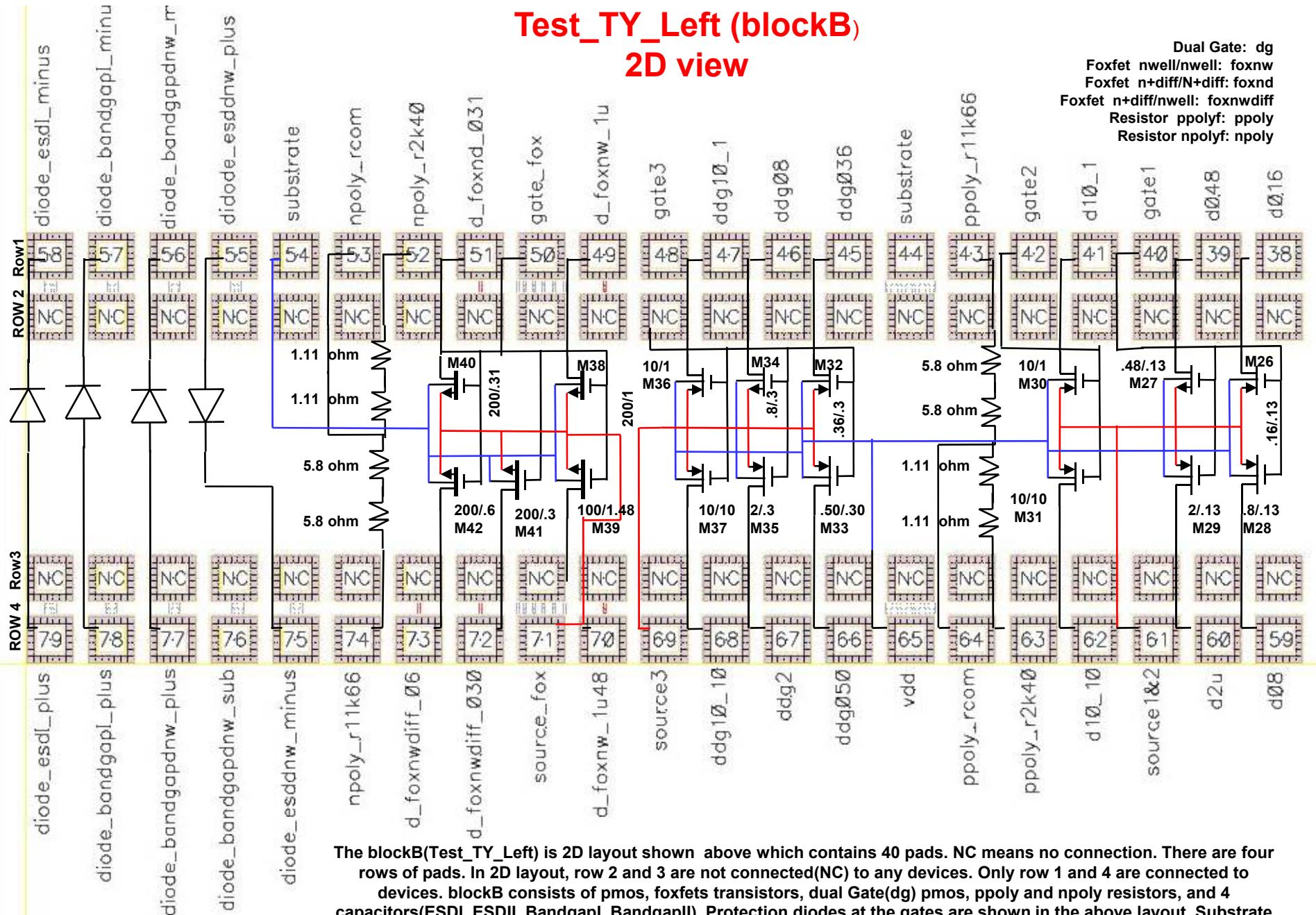
## Pad Assignment for blockA

Pin#	Devices
1	Drain NMOS 0.16/0.13
2	Drain NMOS 0.48/0.13
3	Common Gate NMOS W array(L=.13)
4	Drain NMOS 0.8/0.13
5	Drain NMOS 10/1
6	Common Gate NMOS L array(w=10, L=1 &10) all Zero Vt, ELT, all Triple well with 2.2nm gate oxide
7	Drain Zero Vt NMOS 3/0.42
8	Drain Triple-Well NMOS 0.16/0.13
9	<b>Substrate(Vss)</b>
10	Drain DG NMOS 0.36/0.35
11	Drain DG NMOS 0.8/0.35
12	Drain DG NMOS 10/1
13	Common Gate all DG NMOS
14	Drain DG ELT NMOS 2.34/0.35
15	Drain DG Triple-Well NMOS 0.36/0.35
16	Drain DG Zero Vt ELT NMOS 3.46/1.2
17	Mim_SM cap Bottom (10 pf)
18	Mim_SM cap Top(10 pf)

Pin#	Devices
19	Metal capacitor Top
20	Empty
21	Metal capacitor Bottom
22	Drain NMOS 0.32/0.13
23	Drain NMOS 0.64/0.13
24	Common Source NMOS W array(L=.13), all zeroVt, ELT, & all Triple well with 2.2nm gate oxide
25	Drain NMOS 0.64/0.13
26	Drain NMOS 10/10
27	Drain ELT NMOS 2.17/0.13
28	Drain Zero Vt ELT NMOS 4.22/0.42
29	Drain Triple-Well NMOS 1/0.13
30	<b>Common Vdd</b>
31	Drain DG NMOS 0.50/0.35
32	Drain DG NMOS 2/0.35
33	Drain DG NMOS 10/10
34	Common Source all DG NMOS
35	Drain DG Zero Vt NMOS 2.94/1.2
36	Drain DG Triple-Well NMOS 1/0.35
37	Drain DG NMOS 0.36/0.35 with metal filling on top

## Test\_TY\_Left (blockB) 2D view

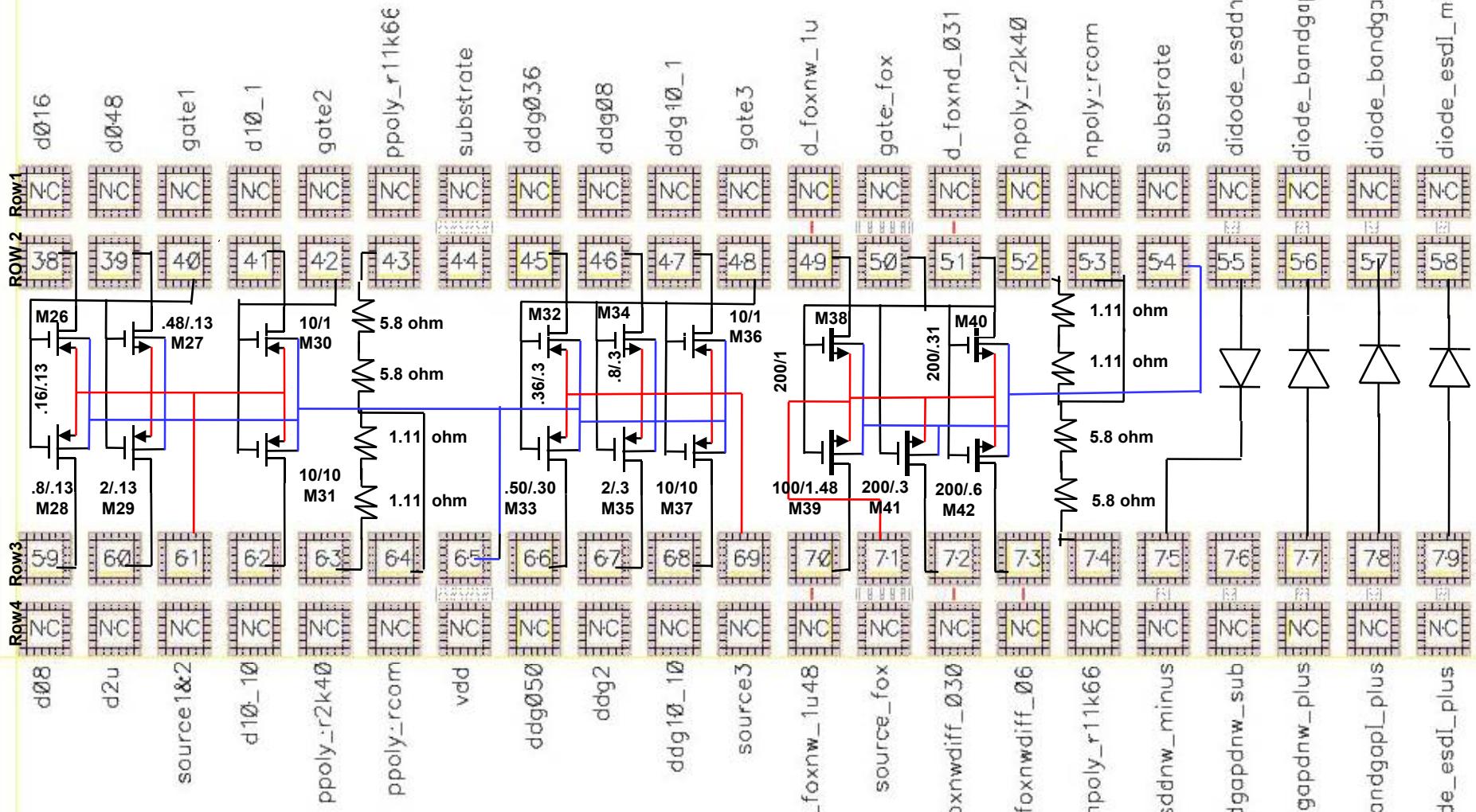
**Dual Gate: dg**  
**Foxfet nwell/nwell: foxnw**  
**Foxfet n+diff/N+diff: foxnd**  
**Foxfet n+diff/nwell: foxnwdiff**  
**Resistor ppoly: ppoly**  
**Resistor npoly: npoly**



The blockB(Test\_TY\_Left) is 2D layout shown above which contains 40 pads. NC means no connection. There are four rows of pads. In 2D layout, row 2 and 3 are not connected(NC) to any devices. Only row 1 and 4 are connected to devices. blockB consists of pmos, foxfets transistors, dual Gate(dg) pmos, ppoly and npoly resistors, and 4 capacitors(ESDI, ESDII, BandgapI, BandgapII). Protection diodes at the gates are shown in the above layout. Substrate is connected to protection diode.

Dual Gate: dg  
 Foxfet nwell/nwell: foxnw  
 Foxfet n+diff/N+diff: foxnd  
 Foxfet n+diff/nwell: foxnwdiff  
 Resistor ppolyf: ppoly  
 Resistor npolyf: npoly

## Test\_TY\_Right (blockB) 2D View



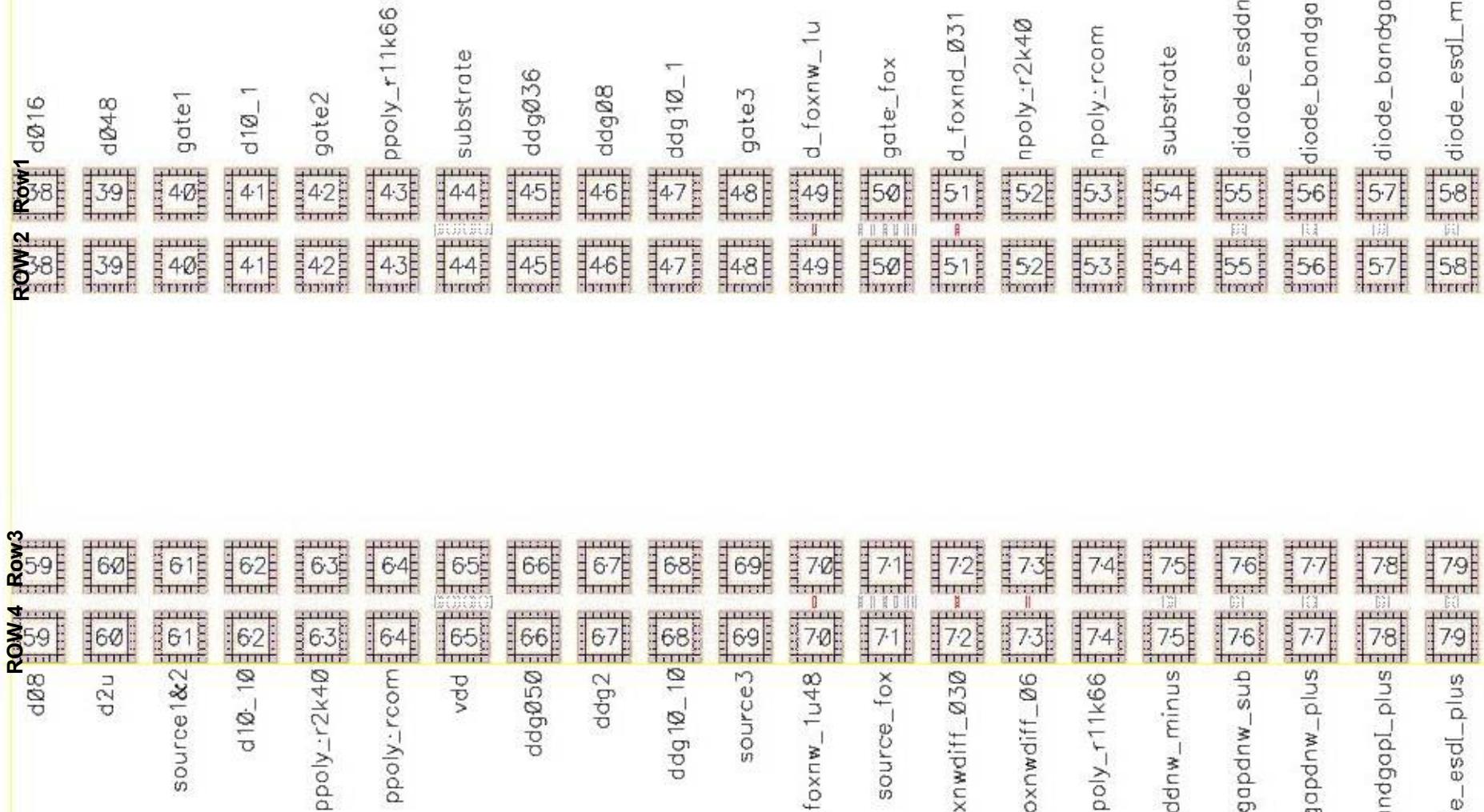
The blockB(Test\_TY\_Right) is 2D layout shown above which is mirror of blockB(Test\_TY\_Left). In this layout, row 2 & 3 are connected to devices and unconnected rows are 1 & 4. NC means no connection. Pin name & devices are exact same as blockB(Test\_Ty\_left). blockB consists of pmos, dual Gate(dg) pmos, ppoly and npoly resistors, and 4 diodes(ESDI, ESDII, BandgapI, and BandgapII). Protection diodes at the gates are not shown in the above layout. Substrate is connected to protection diode.

	ROW 1	ROW 2	ROW 3	ROW 4	
diode_esdl_plus	58 57 57	55 56 56	55 54 55	55 54 53	diode_bandgap[ minus plus]
diode_bandgapnw_minus	58 57 57	55 56 56	55 54 55	55 54 53	diode_bandgapdnw_minus diode_esddnw_plus
diode_bandgapnw_sub	58 57 57	55 56 56	55 54 55	55 54 53	substrate
diode_esdl_minus	58 57 57	55 56 56	55 54 55	55 54 53	npoly_rcom
npoly_r11k66	79 78 78	77 77 77	76 76 76	75 75 75	d_foxnwdiff_06
d_foxnwdiff_030	79 78 78	77 77 77	76 76 76	75 75 75	d_foxnwdiff_030
source_fox	79 78 78	77 77 77	76 76 76	75 75 75	source3
d_foxnw_1u48	79 78 78	77 77 77	76 76 76	75 75 75	d_foxnw_1u
source3	79 78 78	77 77 77	76 76 76	75 75 75	gate3
ddg10_10	79 78 78	77 77 77	76 76 76	75 75 75	ddg10_1
ddg2	79 78 78	77 77 77	76 76 76	75 75 75	ddg08
ddg050	79 78 78	77 77 77	76 76 76	75 75 75	ddg036
vdd	79 78 78	77 77 77	76 76 76	75 75 75	substrate
ppoly_rcom	79 78 78	77 77 77	76 76 76	75 75 75	ppoly_r11k66
ppoly_r2k40	79 78 78	77 77 77	76 76 76	75 75 75	gate2
d10_10	79 78 78	77 77 77	76 76 76	75 75 75	d10_1
source1&2	79 78 78	77 77 77	76 76 76	75 75 75	gate1
d2u	79 78 78	77 77 77	76 76 76	75 75 75	d0.48
d08	79 78 78	77 77 77	76 76 76	75 75 75	d0.16

**Test\_TY\_Right(blockB) flipped on top  
of Test\_TY\_Left(blockB)**  
**3D View**

3D layout of blockB is shown above . where right tier flipped on top of left tier which means row of 1 & 4 pads are connected to circuit. In the case of left tier flipped on top of right tier then row of 2 & 3 are connected to circuit. Either case, one can test the circuit by accessing row 1 & 4 or row 2 & 3. Notice that chip Id at lower right corner.

## Test\_TY\_Right(blockB) flipped on top of Test\_TY\_Left(blockB) 3D View



3D layout of blockB is shown above . where left tier flipped on top of right tier which means row of 2 & 3 pads are connected to circuit. In the case of right tier flipped on top of left tier then row of 1 & 4 are connected to circuit. Either case, one can test the circuit by accessing row 1 & 4 or row 2 & 3. Notice that chip Id at lower left corner.

## Pad Assignment for blockB

Pin#	Devices
38	Drain PMOS 0.16/0.13
39	Drain PMOS 0.48/0.13
40	Common Gate PMOS W array(L=.13)
41	Drain PMOS 10/1
42	Common Gate PMOS L array(w=10,L=1&10)
43	ppoly resistor 11.66k ohm
44	<b>Substrate(Vss)</b>
45	Drain DG PMOS 0.36/0.30
46	Drain DG PMOS 0.8/0.30
47	Drain DG PMOS 10/1
48	Common Gate all DG PMOS
49	Drain FOXFET Nwell 200/1
50	Common Gate FOXFETs
51	Drain FOXFET Ndifusion 200/0.31
52	Npoly resistor 2.40k ohm
53	Common Terminal for 2 npoly resistors (2.40K +11.66K ohm)
54	Substrate for npoly resistors
55	Anode deep nwell diode

Pin#	Devices
56	Cathode DNW bandgap diode
57	Cathode bandgap diode
58	Cathode diode
59	Drain PMOS 0.8/0.13
60	Drain PMOS 2/0.13
61	Common Source PMOS
62	Drain PMOS 10/10
63	Poly resistor 2.4k ohm
64	Common terminal for 2 ppoly resistors(11.66k + 2.4k ohm)
65	<b>Common Vdd</b>
66	Drain DG PMOS 0.50/0.3
67	Drain DG PMOS 2/0.3
68	Drain DG PMOS 10/10
69	Common Source DG PMOS
70	Drain FOXFET Nwell 100/1.48
71	Common Source FOXFETs
72	Drain FOXFET NW/n+diff L=.3
73	Drain FOXFET NW/n+diff L=.6
74	Npoly resistor 11.66k ohm

Pin#	Devices
75	Cathode Deep NW diode
76	Deep NW bandgap diode Substrate
77	Anode deep NW bandgap diode
78	Anode bandgap diode
79	Anode diode

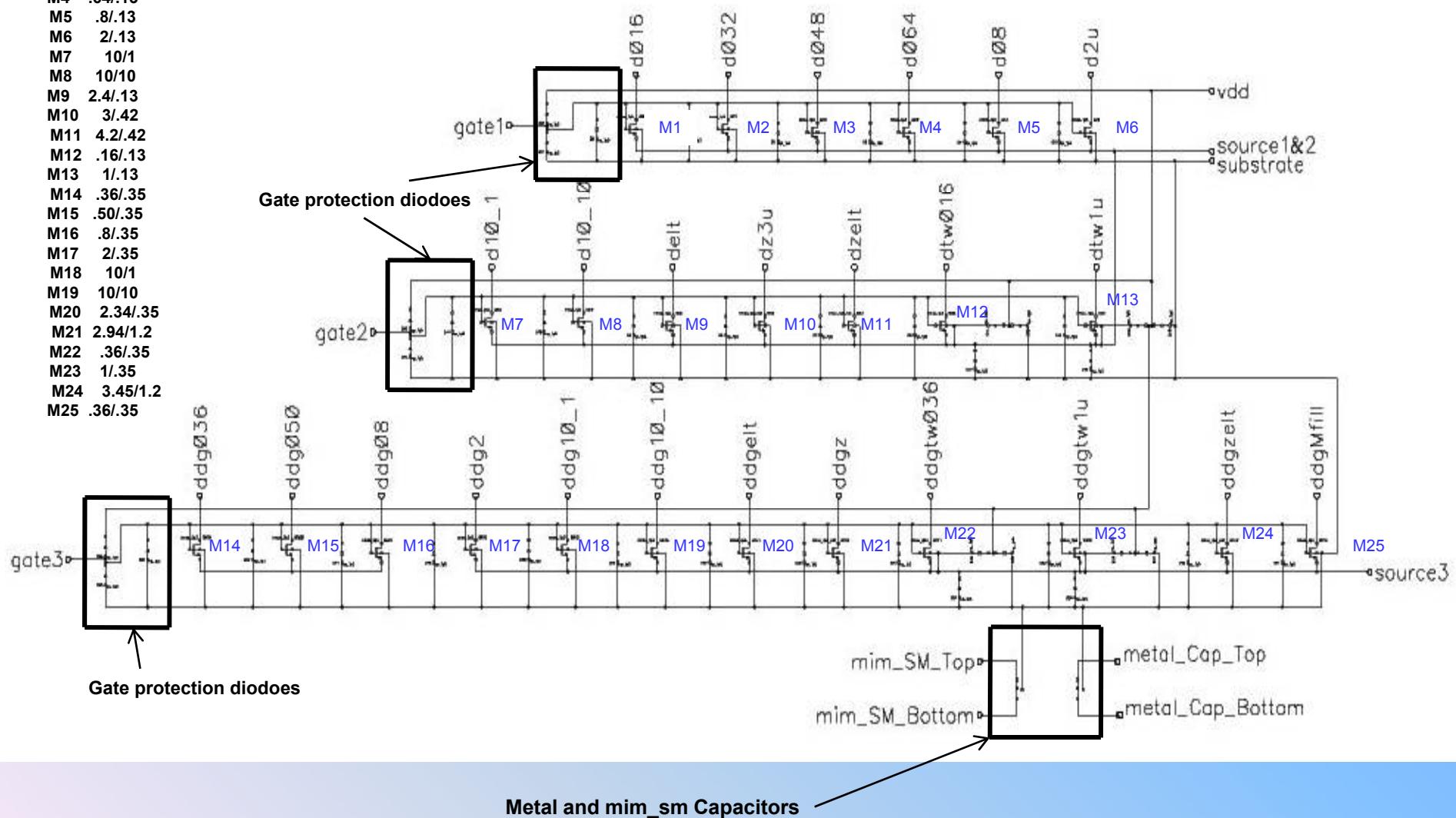
## Summary of Fermi Test Circuit Devices with size and number of pads

Device	Size	Pad count	Numbers
<b>Gate Oxide Devices for 1.5V 2.8nm (model) &amp; 2.6nm(physical)</b>			Transistors
NMOS W array, L=0.13	W=0.16, 0.32, 0.48, 0.64, 0.8, 2	8 (s, g, 6xd)	M1,M2,M3,M4,M5,M6
NMOS L array, W=10	L=1, 10	3 (g, 2xd)	M7,M8
NMOS edgeless (ELT)	W=2.17, L=0.13	1 (d)	M9
NMOS ZVt	W=3, L=0.42	1 (d)	M10
NMOS ZVt edgeless (ELT)	W=4.2, L=0.42	1 (d)	M11
NMOS triple well array, L=0.13	W=0.16, 1	2 (2xd)	M12,M13
PMOS W array, L=0.13	W=0.16, 0.48, 0.8, 2	6 (s, g, 4xd)	M26,M27
PMOS L array, W=10	L=1, 10	3 (g, 2xd)	M30,M31
		<b>25</b>	
<b>Gate Oxide Devices for 3.3V 7.0nm (model) &amp; 6.5nm(physical)</b>			
NMOS W array, L=0.35	W=0.36, 0.50, 0.8, 2	6 (s, g, 4xd)	M14,M15,M16,M17
NMOS L array, W=10	L=1, 10	2 (2xd)	M18,M19
NMOS edgeless (ELT)	W=2.34, L=0.35	1 (d)	M20
NMOS ZVt	W=2.94, L=1.2	1 (d)	M21
NMOS ZVt edgeless (ELT)	W=3.45, L=1.2	1 (d)	M24
NMOS triple well array, L=0.35	W=0.36, 1	2 (2xd)	M22,M23
NMOS with metal filling on top	W=0.36, L=0.35	1 (d)	M25
PMOS W array, L=0.30	W=0.36, 0.50, 0.8, 2	6 (s, g, 4xd)	M32,M33,M34,M35
PMOS L array, W=10	L=1, 10	2 (2xd)	M36,M37
		<b>22</b>	
<b>Resistors</b>			
npolyf_u , & ppolyf_u	L= 13.2u W=.8u, 3.95u (R=11.66 and 2.40 kΩ respectively)	6	
		<b>6</b>	
		<b>6</b>	
<b>FOXFETs</b>			
Nwell/Nwell foxfet array, W=200	L=0.92, 1.48	3	M38,M39
N+diff/N+diff foxfet, W=200	L=0.18	2	M40
N+diff/Nwell foxfet array, W=200	L=0.3, 0.6	2	M41,M42
		<b>7</b>	
<b>Diodes</b>			
ESDI, ESDII(DNW), BandgapI, & BandgapII(DNW)	Area = 1680 μm <sup>2</sup>	9	
		<b>9</b>	
<b>Capacitors</b>			
Mim_SM, & metal to metal	10pf, 1pf	4	
		<b>4</b>	
<b>Power</b>			
Vdd		2	
Gnd		3	
		<b>5</b>	
<b>Pad Total</b>		<b>78</b>	

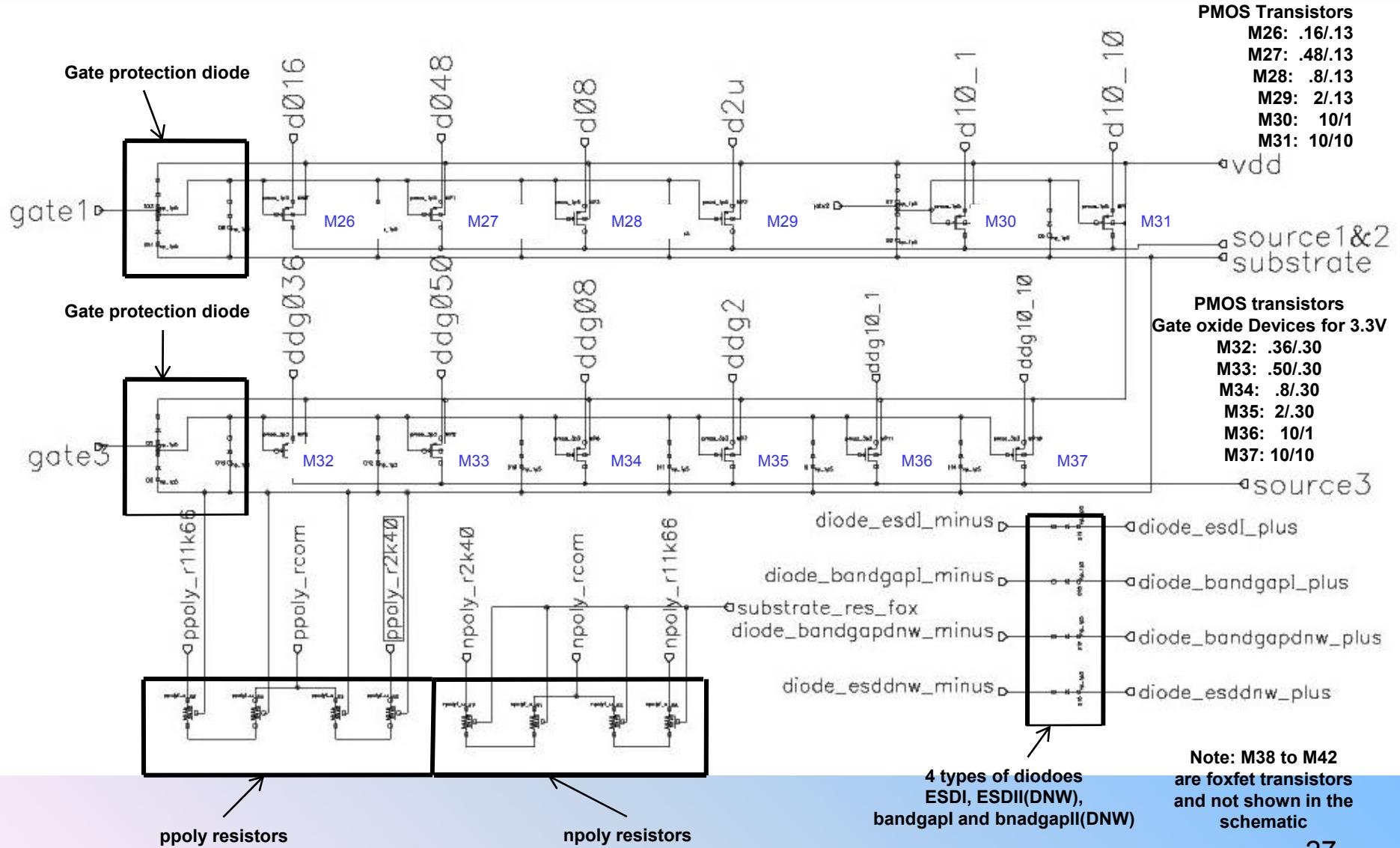
Nmos Transistors

M1	.16/.13
M2	.32/.13
M3	.48/.13
M4	.64/.13
M5	.8/.13
M6	2/.13
M7	10/1
M8	10/10
M9	2.4/.13
M10	3/.42
M11	4.2/.42
M12	.16/.13
M13	1/.13
M14	.36/.35
M15	.50/.35
M16	.8/.35
M17	2/.35
M18	10/1
M19	10/10
M20	2.34/.35
M21	2.94/1.2
M22	.36/.35
M23	1/.35
M24	3.45/1.2
M25	.36/.35

## BlockA Schematic



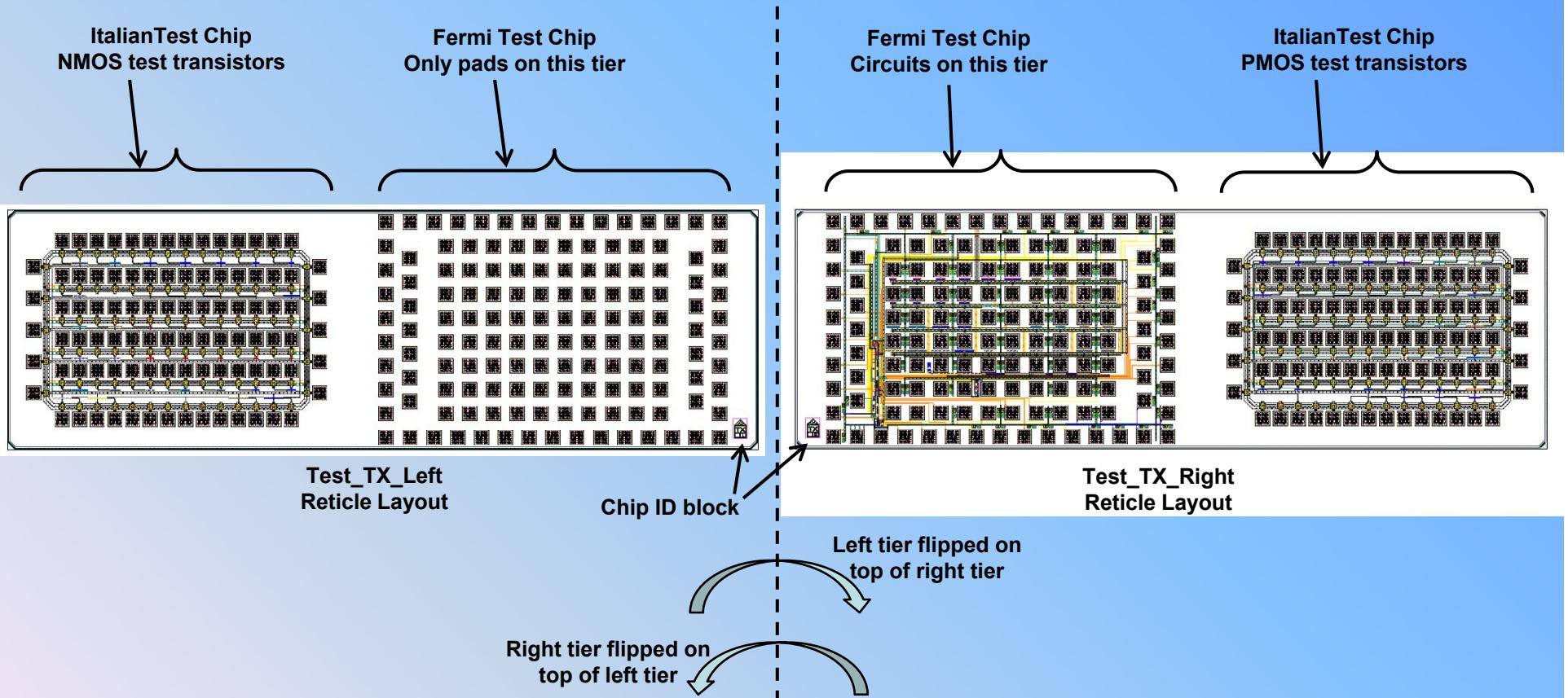
## BlockB Schematic



# Test Circuit TX

- Test TX has transistors for noise, radiation, and cryogenic temperature (using thick gate oxide) measurements.
- TX also has various test circuits for the VIP2b in subreticule I.
- Double Stack pads are used in some locations.

# Test TX (Test Chip X, with Fermi and Italian test ckts.)



## Italian test chips

These chips have no M5-M6 or ReDistribution Layer vias, therefore no 2D testing is possible, and 3D testing is possible only on the top (thinned) tier.

Left tier on top: NMOS test transistors

Right tier on top: PMOS test transistors

## Fermi test chip

Circuits on the right tier only

Only pads (no circuits) on the left tier

Tiers are interconnected (M5-M6 vias exist)

2D testing of right tier is possible (RDL vias exist)

3D, left tier on top: circuits are on bottom (non-thinned) tier

3D, right tier on top: circuits are on top (thinned) tier

## Single Transistors for Noise Measurements on Italian Test Chip X

### “Left” (“Top”) Tier:

#### NMOS

(1P5)

20/.13, 20/.20, 20/.35, 20/.50, 20/.70, 20/1 (5u finger length)  
100/.13, 100/.35 (5u finger length)  
200/.13, 200/.20, 200/.35, 200/.50, 200/.70, 200/1 (5u finger length)  
600/.13, 600/.35 (6u finger length)  
1000/.13, 1000/.20, 1000/.35, 1000/.50, 1000/.70, 1000/1, 1000/1.2 (10u finger length)

**(LVT)**  
1000/.35, 1000/.50, 1000/.70, 1000/1

**(3P3)**  
1000/.35, 1000/.50, 1000/.70, 1000/1, 1000/1.2

**(NAT)**  
1000/.35, 1000/.50, 1000/.70, 1000/1, 1000/1.2

**(3P3\_NAT)**  
1000/1.2

“NMOS” tier

### “Right” (“Bottom”) Tier:

#### PMOS

(1P5)

20/.13, 20/.20, 20/.35, 20/.50, 20/.70, 20/1  
100/.13, 100/.35  
200/.13, 200/.20, 200/.35, 200/.50, 200/.70, 200/1  
600/.13, 600/.35  
1000/.13, 1000/.20, 1000/.35, 1000/.50, 1000/.70, 1000/1

**(LVT)**  
1000/.35, 1000/.50, 1000/.70, 1000/1

**(3P3)**  
1000/.35, 1000/.50, 1000/.70, 1000/1

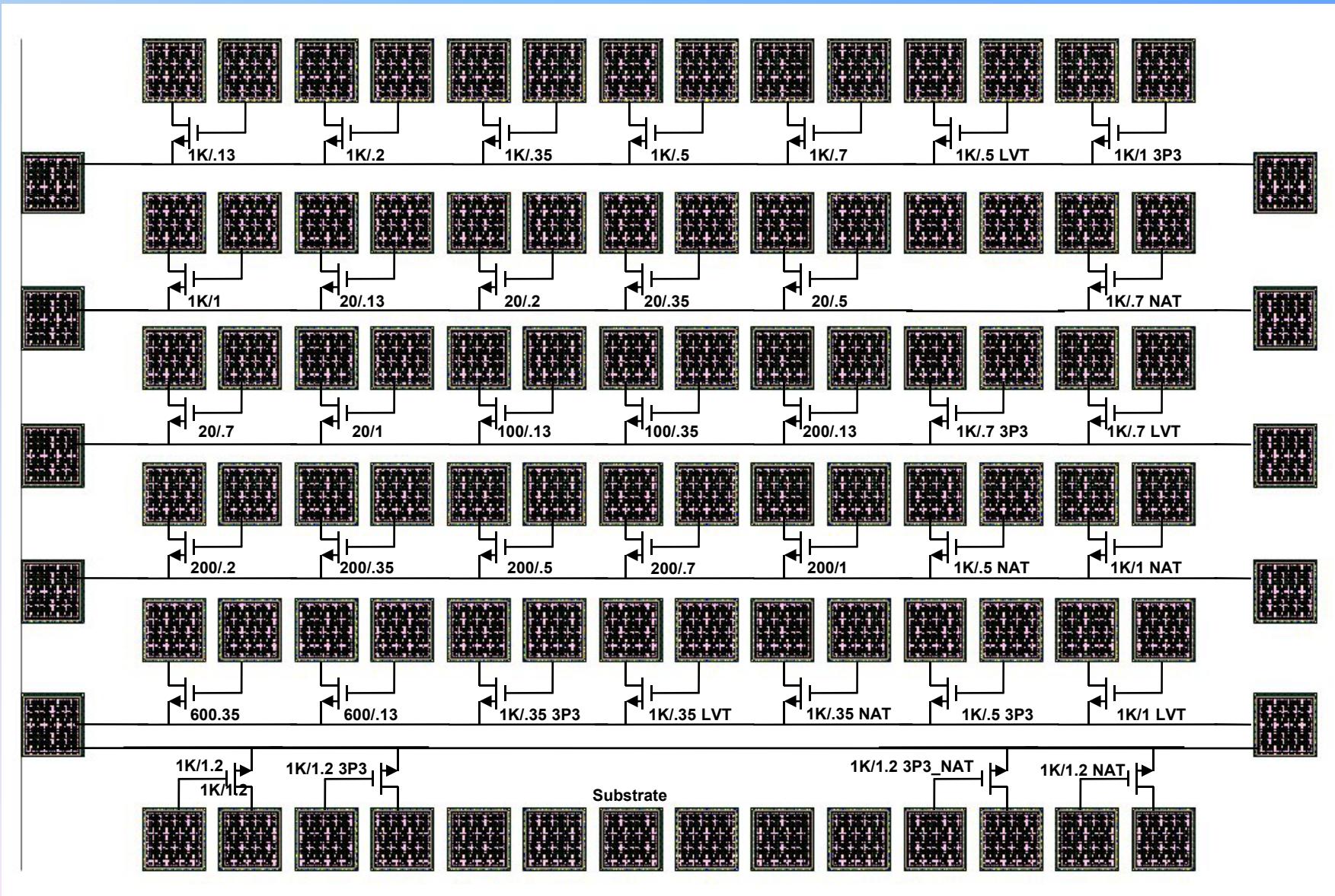
“PMOS” tier  
(includes some NMOS)

#### NMOS

200/.13, 200/.35 (enclosed layout, finger length = 10u)  
600/.13, 600/.35 (enclosed layout, finger length = 10u)  
1000/.13, 1000/.35, 1000/.5 (enclosed layout, finger length = 10u)  
1000/.35 (enclosed layout, finger length = 5u)  
1000/.35 (enclosed layout, finger length = 20u)

# ItalianTest Chip X Pinout

(With left tier on top; NMOS test transistors)



← Fermi Test Chip  
and left tier chip ID block

# ItalianTest Chip X Pinout

(With right tier on top; PMOS test transistors)



f5 = gate finger length of 5 $\mu$   
f20 = gate finger length of 20 $\mu$   
EL = enclosed layout

NMOS transistors

32  
Fermi Test Chip →  
and right tier chip ID block

## Single Transistors for Noise Measurements on Fermi Test Chip X

(same transistors on both tiers)

### **NMOS** **(1P5)**

1000/.13, 1000/.20, 1000/1, 1000/1.2

80/.13 (4 varieties: 1 finger, 2 fingers, 8 fingers, and 8 fingers with non-minimum drain length)

80/.50 (4 varieties: 1 finger, 2 fingers, 8 fingers, and 8 fingers with non-minimum drain length)

### **(LVT)**

1000/.50

### **(3P3)**

1000/.35, 1000/1, 1000/1.2

80/.35 (4 varieties: 1 finger, 2 fingers, 8 fingers, and 8 fingers with non-minimum drain length)

80/.70 (4 varieties: 1 finger, 2 fingers, 8 fingers, and 8 fingers with non-minimum drain length)

### **(NAT)**

1000/.35, 1000/1, 1000/1.2

### **(3P3\_NAT)**

1000/1.2

### **PMOS** **(1P5)**

1000/.13, 1000/.20, 1000/1

80/.13 (3 varieties: 1 finger, 2 fingers, and 8 fingers)

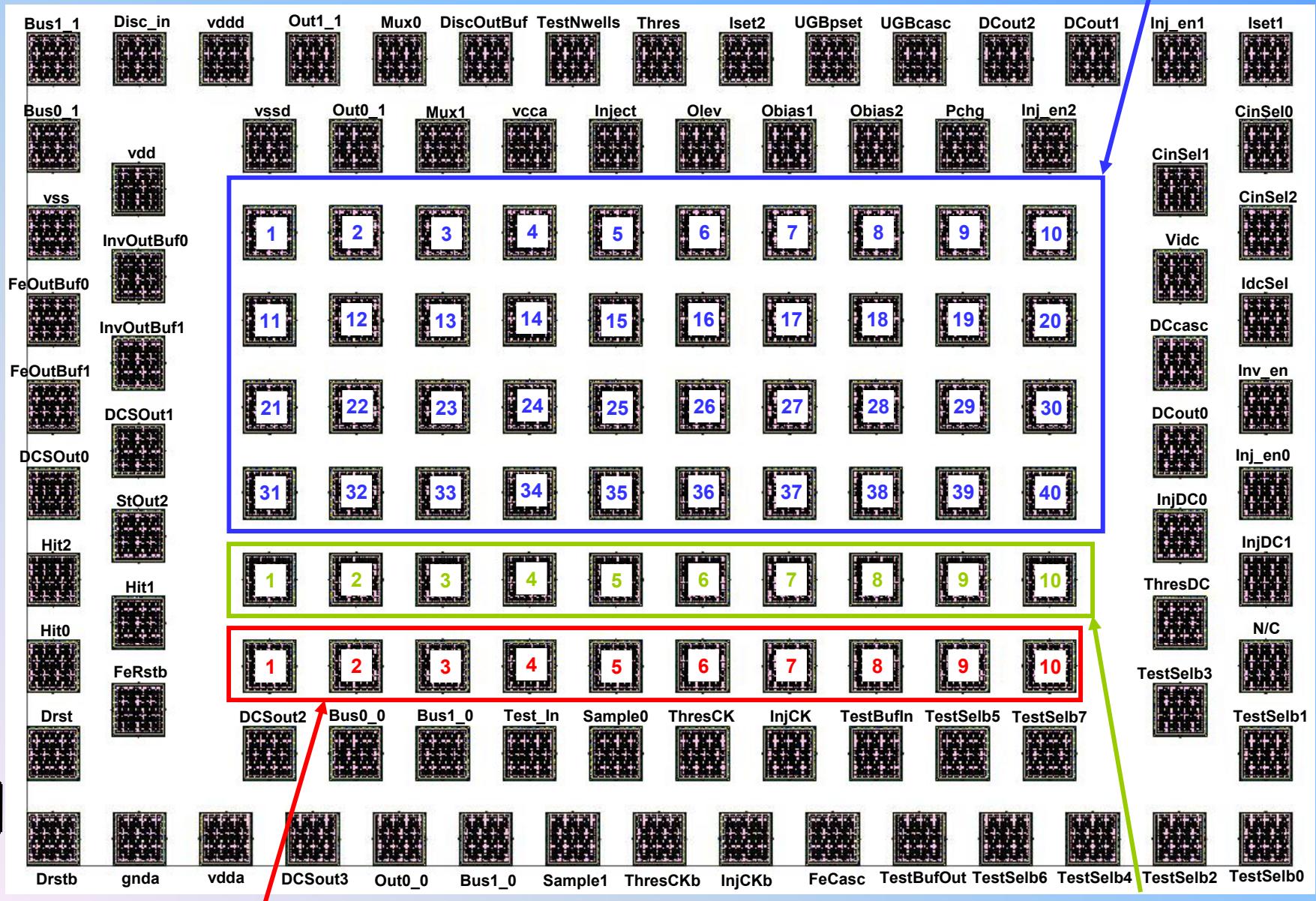
### **(3P3)**

1000/.35, 1000/1

# Fermi Test Chip X Pinout

(With left tier on top; right tier with circuits is on the bottom)

Test transistors:  
Some from Italy,  
Some from Fermilab



DCS test ckt.

Fermi Noise test ckt.

(Mirror this pinout if right tier [with circuits] is on top)

## Fermi Test Chip X Pinout

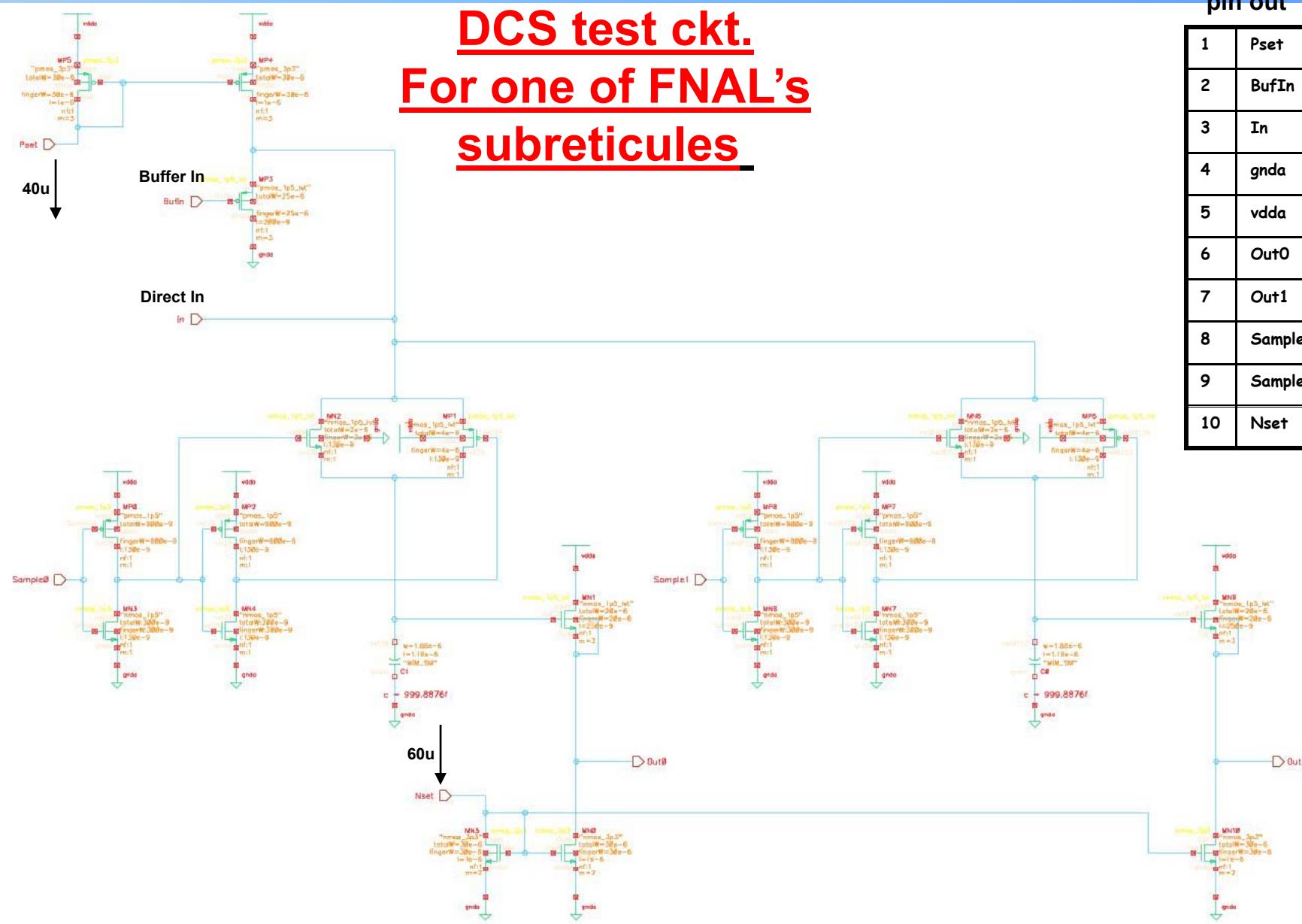
Test Transistors (All NMOS)	
1	1000/.13
2	1000/.20
3	1000/1.0
4	1000/.35_3P3
5	All PMOS sources
6	All PMOS gates
7	1000/1_3P3
8	80/.13, 1 finger
9	80/.13, 2 fingers
10	80/.13, 8 fingers
11	1000/.13
12	1000/.20
13	1000/1
14	1000/.50_LVT
15	All NMOS gates
16	80/.13, 1 finger
17	80/.13, 2 fingers
18	80/.13, 8 fingers
19	80/.13, 8 fingers NMD
20	80/.70_3P3, 1 finger
21	1000/1.0_NAT
22	1000/.35_NAT
23	1000/1.2
24	1000/.35_3P3
25	All NMOS sources
26	80/.5, 1 finger
27	80/.5, 2 fingers
28	80/.5, 8 fingers
29	80/.5, 8 fingers NMD
30	80/.70_3P3, 2 fingers
31	1000/1.2_3P3_NAT
32	1000/1.2_NAT
33	1000/1.2_3P3
34	1000/1.0_3P3
35	80/.35_3P3, 1 finger
36	80/.35_3P3, 2 fingers
37	80/.35_3P3, 8 fingers
38	80/.35_3P3, 8 fingers NMD
39	80/.7_3P3, 8 fingers 35
40	80/.7_3P3, 8 fingers NMD

NMD = Non-Minimum Drain dimension

pin out

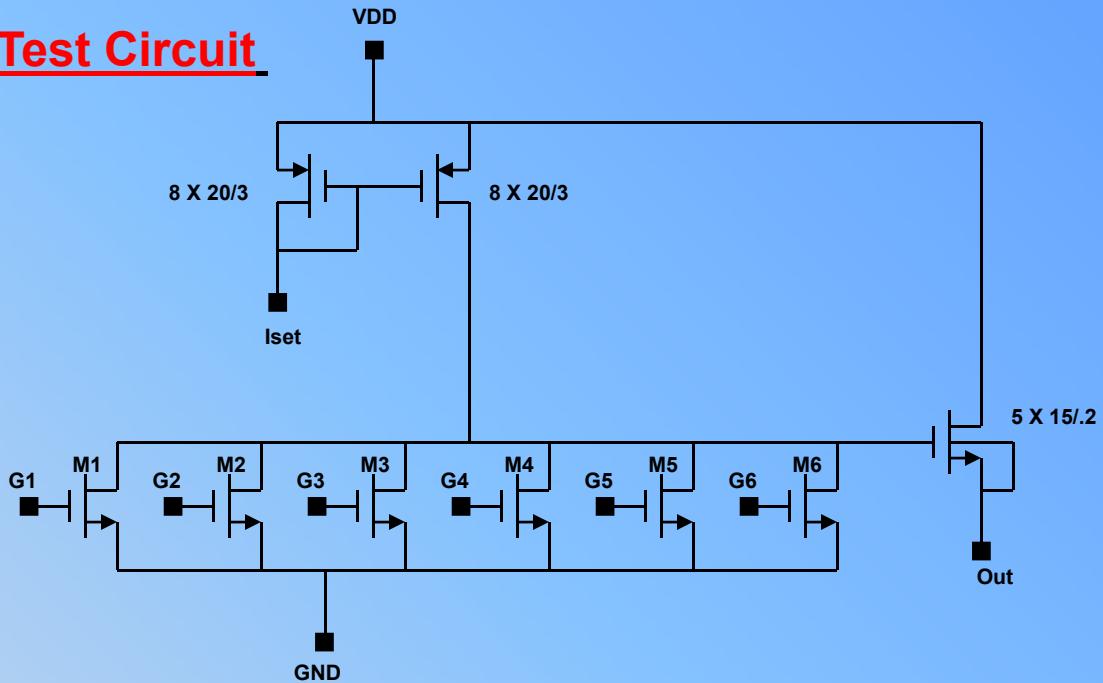
1	Pset
2	BufIn
3	In
4	gnda
5	vdda
6	Out0
7	Out1
8	Sample0
9	Sample1
10	Nset

## DCS test ckt. For one of FNAL's subreticules



pin out	
1	Iset
2	VDD
3	Out
4	G1
5	G2
6	G3
7	GND
8	G4
9	G5
10	G6

## Fermi Noise Test Circuit



M1: 1000/1.2\_3P3\_NAT

M2: 1000/1.2\_NAT

M3: 1000/1.2

M4: 1000/.13

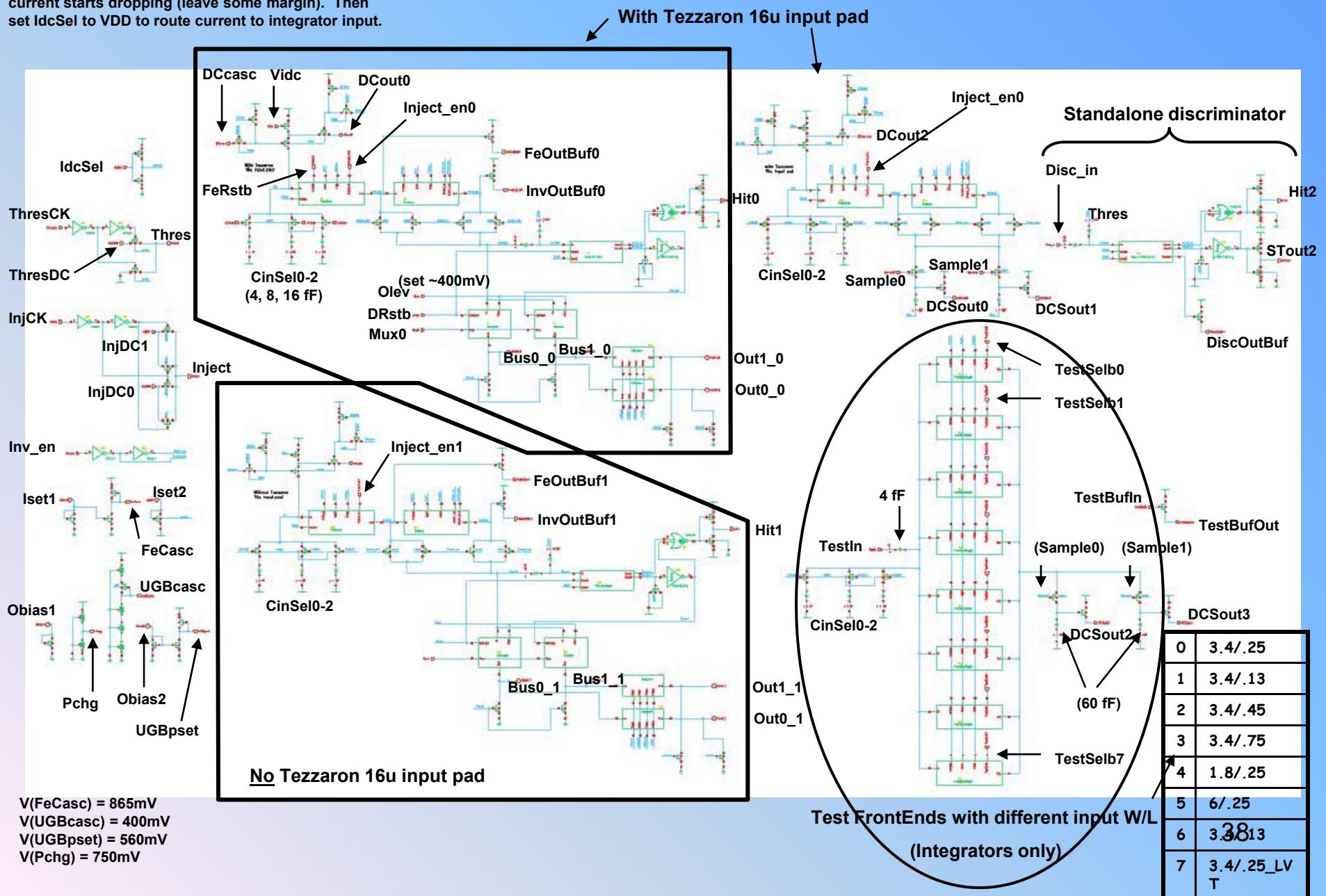
M5: 1000/.5

M6: 1000/.5\_3P3

If IdcSel = 0V: DC test current to DCout pad.  
If IdcSel = VDD: DC test current to integrator input

Set IdcSel to 0, then set Vidc to ~1-1.2V to set DC test current, with DCCasc ~1V. Adjust DCCasc higher until current starts dropping (leave some margin). Then set IdcSel to VDD to route current to integrator input.

## Fermi Test Circuits for VIP2b



# Summary

- The numerous test circuits on various subreticules in addition to those on TX and TY should provide a wealth of test information to be shared within the consortium.